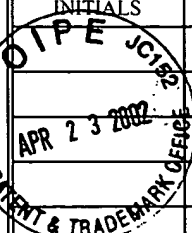
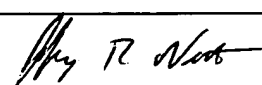
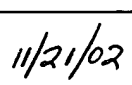


<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <b>(PTO-1449)</b>				ATTY. DOCKET NO. <b>50006-128</b>		SERIAL NO. <b>09/977,994</b>	
				APPLICANT <b>Makoto NAGATA, et al.</b>			
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<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
							
<b>FOREIGN PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
JRw	M. Nagata, et al, "Measurements and Analyses of Substrate Noise Waveform in Mixed-Signal IC Environment" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 19, No. 6, June 2000, pages 671 - 678						
JRw	M. Nagata, et al, Measurements and Analyses of Substrate Noise Waveform in Mixed-Signal IC Environment" Proceedings of the IEEE 1999 Custom Integrated Conference, May 1999, pages 575 - 578						
JRw	M. Nagata, et al, "Substrate Crosstalk Analysis in Mixed Signal CMOS Integrated Circuits" Asia and South Pacific Design Automation Conference 2000 With EDA Technofair 2000. January 2000, pages 623 - 629						
JRw	M. Nagata, et al, "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits" Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, May 2000, Vol. 36, No. 3, pages 539 - 549						
<del>          </del>	<del>K. Shimazaki, et al "LEMINGS: LSI's EMI-Noise Analysis With Gate Level Simulator" Proceedings IEEE 2000 First International Symposium on Quality Electronic Design, March 2000, pages 1 - 8</del>						
EXAMINER				DATE CONSIDERED			
							

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.